

CIRCUIT AND METHOD FOR SUPPORTING MISALIGNED ACCESSES
IN THE PRESENCE OF SPECULATIVE LOAD INSTRUCTIONS

ABSTRACT OF THE DISCLOSURE

There is disclosed a data processor comprising: 1) an
5 instruction execution pipeline comprising N processing stages for
executing a load instruction; 2) a status register for storing a
modifiable configuration value, the modifiable configuration value
having a first value indicating the data processor is capable of
executing a misaligned access handling routine and a second value
10 indicating the data processor is not capable of executing a
misaligned access handling routine; 3) a misalignment detection
circuit for determining if the load instruction performs a
misaligned access to a target address of the load instruction and,
in response to a determination that the load instruction does
15 perform a misaligned access, generating a misalignment flag;
and 4) exception control circuitry capable of detecting the
misalignment flag and in response thereto determining if the
modifiable configuration value is equal to the first value.